

FEATURES

- Operates from 1.65 V to 3.6 V supply rails
- Unidirectional signal path
- Up/down level translation
- Ultracompact 6-lead SOT-66 and SOT-23 packages
- Output short-circuit protection
- LVTTTL-/CMOS-compatible inputs

APPLICATIONS

- Level translation in
 - PDA's
 - Handsets
 - MP3 players

GENERAL DESCRIPTION

The ADG3231¹ is a single-channel level translator designed on a submicron process that is guaranteed to operate over the 1.65 V to 3.6 V supply range. The device can be used in applications requiring communication between digital devices operating from multiple supply voltages. The logic levels on each side of the device are set by the two supply voltages, V_{CC1} for A and V_{CC2} for Y. The signal path is unidirectional, meaning data can flow only from A to Y.

The ADG3231 can operate with any combination of V_{CC1} and V_{CC2} supply voltages within the 1.65 V to 3.6 V range, allowing the part to perform either up ($V_{CC1} < V_{CC2}$) or down ($V_{CC1} > V_{CC2}$) level translation. The output stage is protected against current overload, which can occur when the Y pin is accidentally shorted to the V_{CC2} or GND rails.

FUNCTIONAL BLOCK DIAGRAM

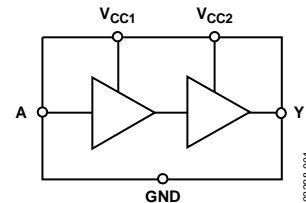


Figure 1.

The ADG3231 is available in ultracompact packages, the SOT-66 (1.65 mm × 1.66 mm × 0.57 mm) and the SOT-23 (2.8 mm × 2.9 mm × 1.3 mm), making the part ideal for applications where space is critical.

PRODUCT HIGHLIGHTS

1. Up/down level translation.
2. Guaranteed to operate with any supply combination within the 1.65 V to 3.6 V range.
3. Output short-circuit protection.
4. Available in ultracompact SOT-66 and SOT-23 packages.

¹ Patent pending.

Rev. B

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REVISION HISTORY

5/06—Rev. A to Rev. B

Deleted Figure 11 and Figure 12.....	7
Changes to Ordering Guide	10

12/04—Rev. 0 to Rev. A

Updated Format	Universal
Added SOT-66 Package	Universal
Change to Data Sheet Title.....	1
Changes to Features, Applications, General Description and Product Highlights Sections	1
Added Patent Information	1

Changes to Figure 1.....	1
Changes to Table 1.....	3
Changes to Figure 2 and Figure 3.....	3
Deleted TPC 1 to TPC 6	6
Changes to Figure 13 through Figure 20.....	7
Changes to Theory of Operation Section.....	9
Updated Outline Dimensions	10
Changes to Ordering Guide	10

5/03—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC1} = V_{CC2} = 1.65\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted. Temperature range for the B version is -40°C to $+85^{\circ}\text{C}$.

Table 1.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
LOGIC INPUTS/OUTPUTS						
Input High Voltage ²	V_{IH}	$V_{CC1} = 3.0\text{ V to }3.6\text{ V}$	1.35			V
		$V_{CC1} = 2.3\text{ V to }2.7\text{ V}$	1.35			V
		$V_{CC1} = 1.65\text{ V to }1.95\text{ V}$	$0.65 V_{CC1}$			V
Input Low Voltage ²	V_{IL}	$V_{CC1} = 3.0\text{ V to }3.6\text{ V}$			0.8	V
		$V_{CC1} = 2.3\text{ V to }2.7\text{ V}$			0.7	V
		$V_{CC1} = 1.65\text{ V to }1.95\text{ V}$			$0.35 V_{CC1}$	V
Output High Voltage	V_{OH}	$I_{OH} = -100\ \mu\text{A}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$	2.4			V
		$I_{OH} = -100\ \mu\text{A}$, $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$	2.0			V
		$I_{OH} = -100\ \mu\text{A}$, $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$	$V_{CC2} - 0.45$			V
		$I_{OH} = -4\text{ mA}$, $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$	2.0			V
		$I_{OH} = -4\text{ mA}$, $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$	$V_{CC2} - 0.45$			V
		$I_{OH} = -8\text{ mA}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$	2.4			V
Output Low Voltage	V_{OL}	$I_{OL} = 100\ \mu\text{A}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$			0.4	V
		$I_{OL} = 100\ \mu\text{A}$, $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$			0.4	V
		$I_{OL} = 100\ \mu\text{A}$, $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$			0.45	V
		$I_{OL} = 4\text{ mA}$, $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$			0.4	V
		$I_{OL} = 4\text{ mA}$, $V_{CC2} = 1.65\text{ V to }1.95\text{ V}$			0.45	V
		$I_{OL} = 8\text{ mA}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$			0.4	V
SWITCHING CHARACTERISTICS ²						
Propagation Delay, t_{PD} A to Y	t_{PHL} , t_{PLH}	$3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 30\text{ pF}$, see Figure 2		4	6.5	ns
Propagation Delay, t_{PD} A to Y	t_{PHL} , t_{PLH}	$2.5\text{ V} \pm 0.2\text{ V}$, $C_L = 30\text{ pF}$, see Figure 2		4.5	6.5	ns
Propagation Delay, t_{PD} A to Y	t_{PHL} , t_{PLH}	$1.8\text{ V} \pm 0.15\text{ V}$, $C_L = 30\text{ pF}$, see Figure 2		6.5	10.25	ns
Input Leakage Current	I_I	$0 \leq V_{IN} \leq 3.6\text{ V}$			± 1	μA
Output Leakage Current	I_O	$0 \leq V_{IN} \leq 3.6\text{ V}$			± 1	μA
POWER REQUIREMENTS						
Power Supply Voltages	V_{CC1}		1.65		3.6	V
	V_{CC2}		1.65		3.6	V
Quiescent Power Supply Current	I_{CC1}	Digital inputs = 0 V or V_{CC1}			2	μA
	I_{CC2}	Digital inputs = 0 V or V_{CC2}			2	μA

¹ All typical values are at $V_{CC1} = V_{CC2}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

² Guaranteed by design, not subject to production test.

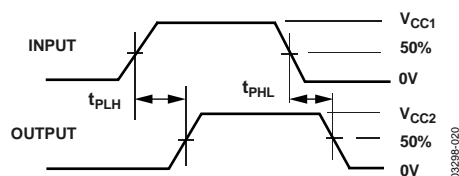


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V _{CC} to GND	-0.3 V to +4.6 V
Input Voltage for A	-0.3 V to V _{CC1} + 0.3 V
DC Output Current	25 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
θ _{JA} Thermal Impedance	
6-Lead SOT-23	229°C/W
6-Lead SOT-66	191°C/W (4-layer board)
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

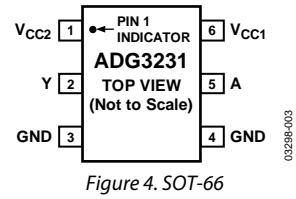
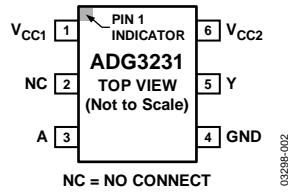


Table 3. Pin Function Descriptions

Pin Number		Mnemonic	Description
SOT-23	SOT-66		
1	6	V _{CC1}	Supply Voltage 1. Can be any supply voltage from 1.65 V to 3.6 V.
2	–	NC	Not internally connected.
3	5	A	Digital Input Referred to V _{CC1} .
4	3, 4	GND	Device Ground Pin.
5	2	Y	Digital Output Referred to V _{CC2} .
6	1	V _{CC2}	Supply Voltage 2. Can be any supply voltage from 1.65 V to 3.6 V.

TYPICAL PERFORMANCE CHARACTERISTICS

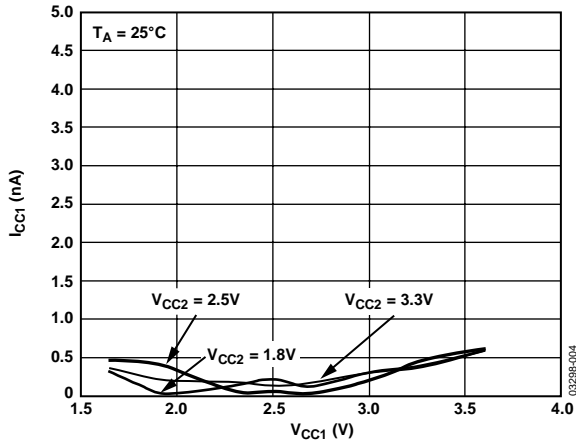


Figure 5. I_{CC1} vs. V_{CC1}

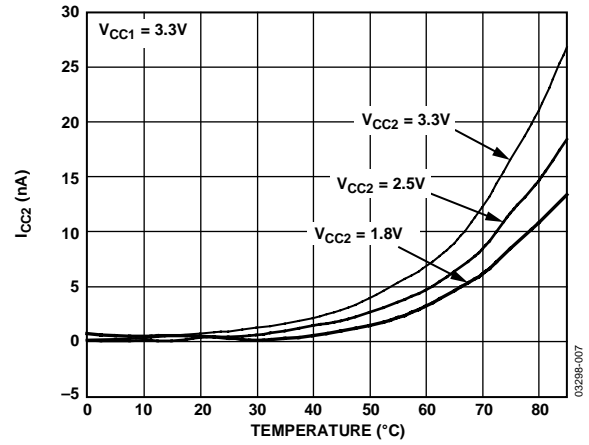


Figure 8. I_{CC2} vs. Temperature

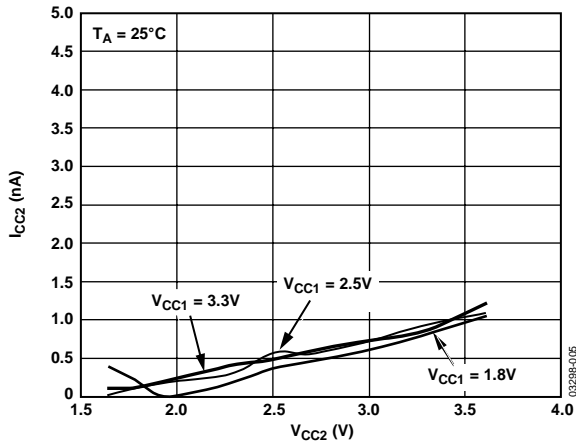


Figure 6. I_{CC2} vs. V_{CC2}

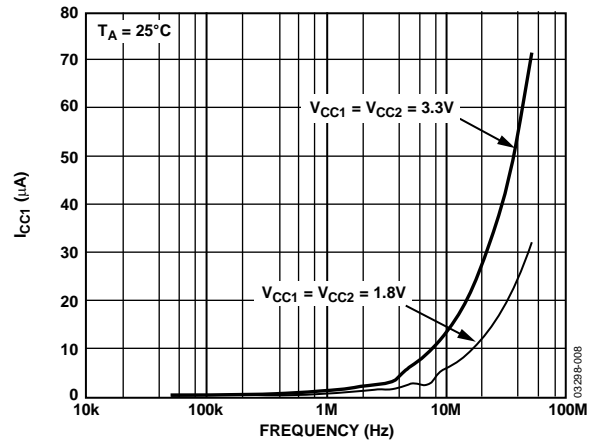


Figure 9. I_{CC1} vs. Frequency

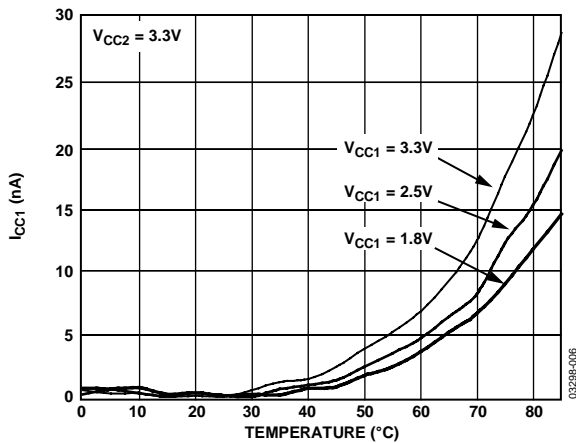


Figure 7. I_{CC1} vs. Temperature

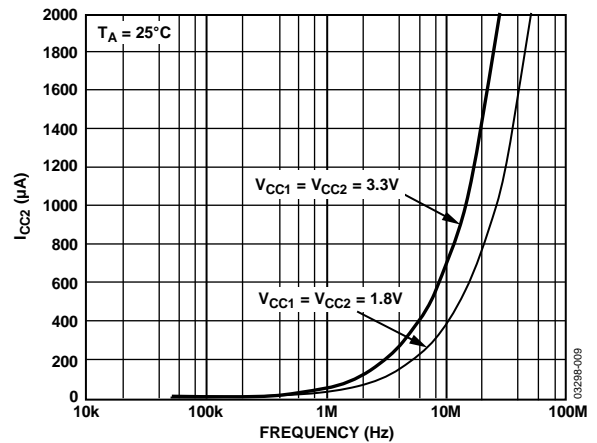


Figure 10. I_{CC2} vs. Frequency

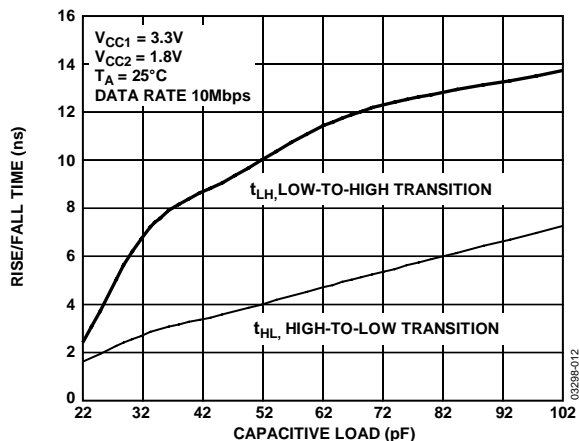


Figure 11. Rise/Fall Time vs. Capacitive Load (3.3 V to 1.8 V Level Translation)

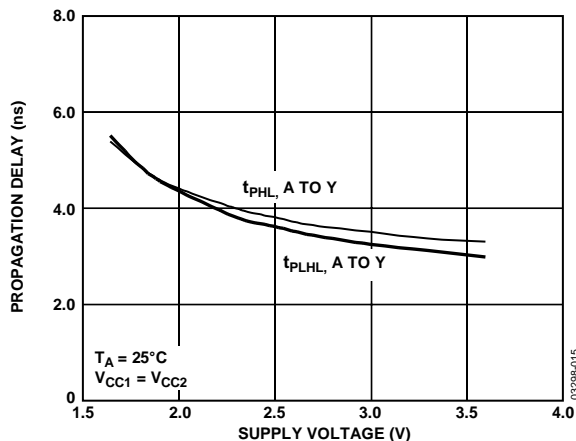


Figure 14. Propagation Delay vs. Supply Voltage

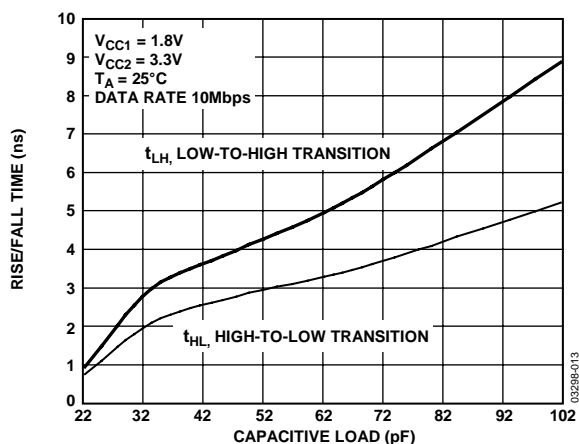


Figure 12. Rise/Fall Time vs. Capacitive Load (1.8 V to 3.3 V Level Translation)

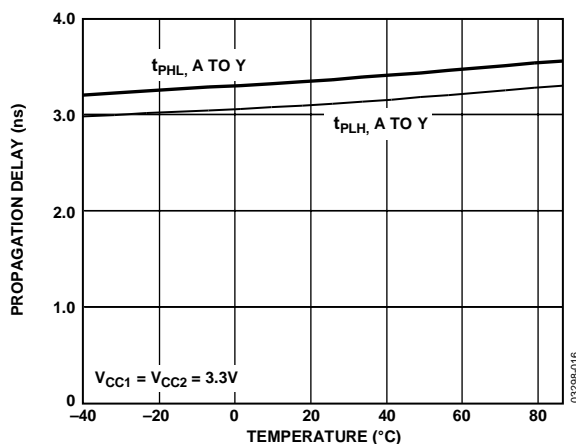


Figure 15. Propagation Delay vs. Temperature

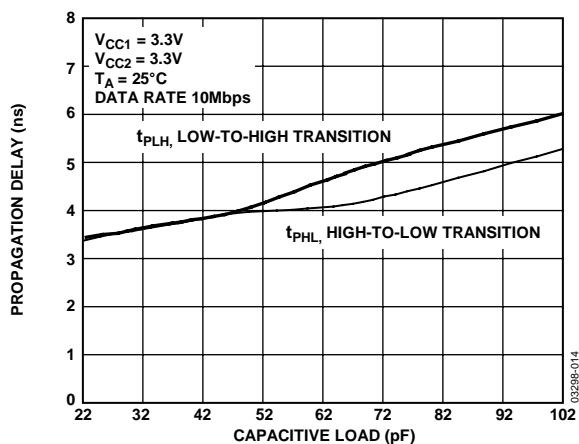


Figure 13. Propagation Delay vs. Capacitive Load

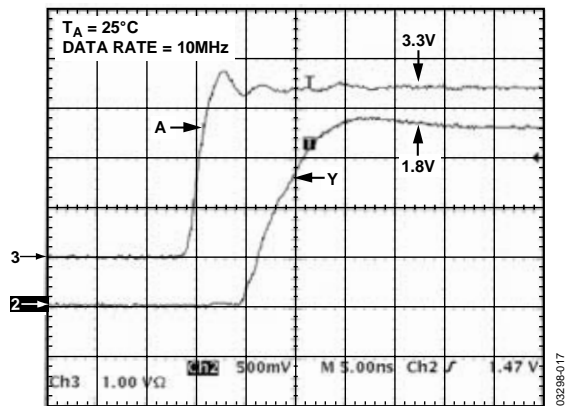


Figure 16. Input/Output $V_{CC1} = 3.3V$, $V_{CC2} = 1.8V$

ADG3231

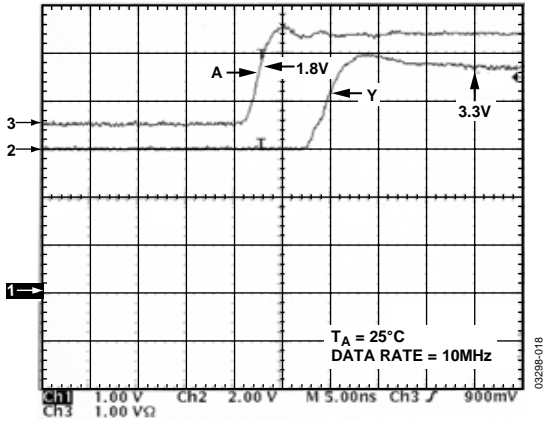


Figure 17. Input/Output $V_{CC1} = 1.8\text{ V}$, $V_{CC2} = 3.3\text{ V}$

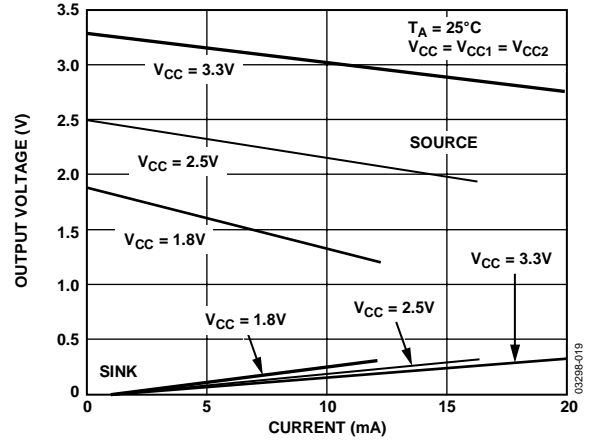


Figure 18. Output Voltage vs. Sink and Source Current

THEORY OF OPERATION

The ADG3231 is a single-channel level translator designed on a submicron process that is guaranteed to operate over the 1.65 V to 3.6 V supply range. The device can be used in applications requiring communication between digital devices operating from multiple supply voltages. The logic levels on each side of the device are set by the two supply voltages, V_{CC1} for A, and V_{CC2} for Y. The signal path is unidirectional, meaning data can flow only from A to Y.

The ADG3231 can operate with any combination of V_{CC1} and V_{CC2} supply voltages within the 1.65 V to 3.6 V range, allowing the part to perform either up ($V_{CC1} < V_{CC2}$) or down ($V_{CC1} > V_{CC2}$) level translation.

By limiting the current delivered into the load, for example, ~ 1.7 mA with $V_{CC2} = 3.6$ V, the output stage is protected against current overload, which can occur when the Y pin is accidentally shorted to the V_{CC2} or GND rails.

The short-circuit protection circuitry works by limiting the output current when the output voltage exceeds V_{OL} ($A = 0$ logic) or is less than V_{OH} ($A = 1$ logic) threshold values specified for the V_{CC2} supply voltage used.

Figure 19 shows a typical application for the ADG3231 where the device performs level translation from V_{CC1} -compatible levels to V_{CC2} -compatible levels to allow proper communication between the two digital devices, DEVICE 1 and DEVICE 2.

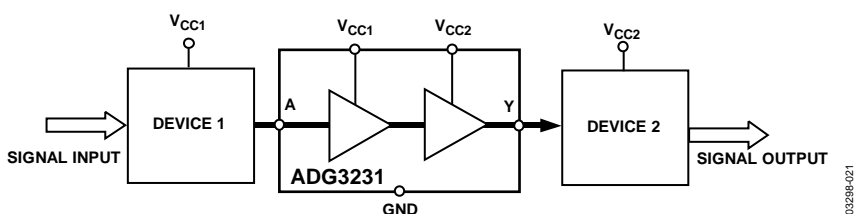
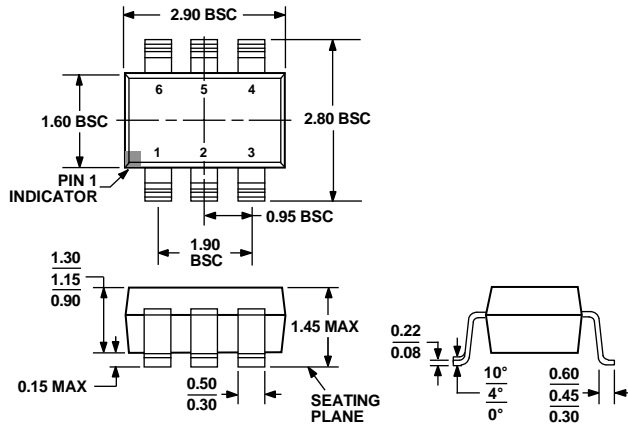


Figure 19. Typical Application of the ADG3231 Level Translator

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 20. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6)

Dimensions shown in millimeters

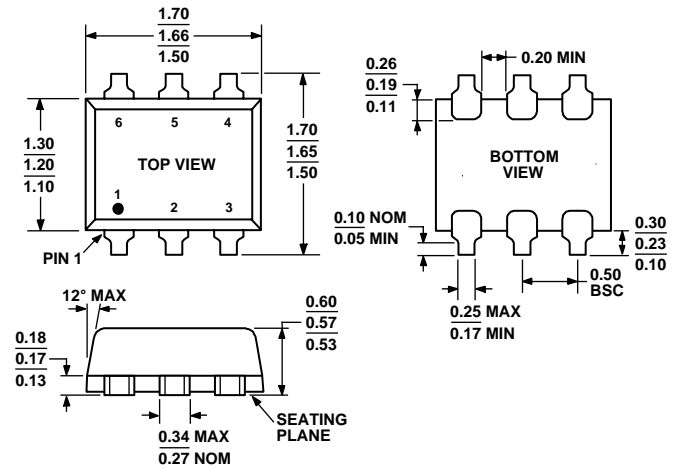


Figure 21. 6-Lead Small Outline Transistor Package [SOT-66] (RY-6-1)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG3231BRJ-REEL	-40°C to +85°C	6-Lead SOT-23	RJ-6	W2B
ADG3231BRJ-REEL7	-40°C to +85°C	6-Lead SOT-23	RJ-6	W2B
ADG3231BRJZ-REEL ¹	-40°C to +85°C	6-Lead SOT-23	RJ-6	W2B #
ADG3231BRJZ-REEL7 ¹	-40°C to +85°C	6-Lead SOT-23	RJ-6	W2B #
ADG3231BRYZ-REEL7 ¹	-40°C to +85°C	6-Lead SOT-66	RY-6-1	01X ²

¹ Z = Pb-free part, # denotes lead-free may be top or bottom marked.

² X = date code.

NOTES

ADG3231

NOTES